

Amendments to the Claims:

1-22. (cancelled)

- 5 23. (new) A method of protecting a memory section from being accessed, the method comprising:
providing a memory being coupled to a microprocessor, the memory having a
memory section to be protected of a particular size;
generating a first memory address by the microprocessor for accessing the memory;
10 shifting the first memory address by an amount being substantially equal to the size
of the memory section to be protected to thereby generate a shifted memory
address being different from the first memory address; and
accessing the memory utilizing the shifted memory address for all memory accesses
by the microprocessor when it is desired to prevent the memory section from
15 being accessed by the microprocessor.
24. (new) The method of claim 23, further comprising preventing the memory section
from being accessed during normal operations of the microprocessor by coupling
the shifted memory address to the memory immediately after the microprocessor
20 has finished booting, and continually coupling the shifted memory address to the
memory for all subsequent normal operations of the microprocessor.
25. (new) The method of claim 24, further comprising:
storing boot code for the microprocessor in the memory section; and
25 booting the microprocessor utilizing the boot code stored in the memory section by
coupling the first memory address to the memory before the microprocessor
begins booting and while the microprocessor is booting.

26. (new) The method of claim 23, further comprising:
storing a value being substantially equal to the size of the memory section to be
protected in a register;
5 shifting the first memory address by the value stored in the register to thereby
generate the shifted memory address;
changing the size of the memory section to be protected to a new size after updating
contents of the memory section;
changing the value stored in the register to a new value corresponding to the new
10 size of the memory section to be protected; and
shifting the first memory address by the new value stored in the register to thereby
generate a new shifted memory address.
27. (new) The method of claim 26, wherein updating contents of the memory section
15 further comprises storing updated boot code for the microprocessor in the memory
section.
28. (new) A method of protecting a memory section from being accessed, the method
comprising:
20 providing a memory being coupled to a microprocessor, the memory having a
memory section to be protected of a particular size;
generating a shifted memory address space of the memory, the shifted memory
address space being shifted by an amount being substantially equal to the size
of the memory section to be protected to thereby move the memory section to
25 be protected outside of the shifted memory address space; and
accessing the memory utilizing shifted memory addresses being within the shifted
memory address space for all memory accesses by the microprocessor when it
is desired to prevent the memory section from being accessed by the

microprocessor.

29. (new) The method of claim 28, further comprising preventing the memory section from being accessed during normal operations of the microprocessor by coupling
5 the shifted memory addresses of the shifted memory address space to the memory immediately after the microprocessor has finished booting, and continually coupling the shifted memory addresses to the memory for all subsequent normal operations of the microprocessor.
- 10 30. (new) The method of claim 29, wherein generating the shifted memory address space includes shifting an original memory address space of the memory by the amount being substantially equal to the size of the memory section to be protected, and the method further comprises:
storing boot code for the microprocessor in the memory section; and
15 booting the microprocessor utilizing the boot code stored in the memory section by coupling un-shifted memory addresses in the original memory address space to the memory before the microprocessor begins booting and while the microprocessor is booting.
- 20 31. (new) The method of claim 28, further comprising:
storing a value being substantially equal to the size of the memory section to be protected in a register;
shifting an original memory address space of the memory by the value stored in the register to thereby generate the shifted memory address space;
25 changing the size of the memory section to be protected to a new size after updating contents of the memory section;
changing the value stored in the register to a new value corresponding to the new size of the memory section to be protected; and

shifting the original memory address space of the memory by the new value stored in the register to thereby generate a new shifted memory address space.

32. (new) The method of claim 31, wherein updating contents of the memory section
5 further comprises storing updated boot code for the microprocessor in the memory section.
33. (new) An electronic system comprising:
a memory having a memory section of a particular size to be protected;
10 a microprocessor being coupled to the memory, for generating a first memory address for accessing the memory; and
an address translator being coupled between the microprocessor and the memory, for shifting the first memory address by an amount being substantially equal to the size of the memory section to be protected to thereby generate a shifted
15 memory address being different from the first memory address;
wherein the shifted memory address outputted by the address translator is coupled to the memory for all memory accesses when it is desired to prevent the memory section from being accessed by the microprocessor.
- 20 34. (new) The electronic system of claim 33, wherein the address translator is further for preventing the memory section from being accessed during normal operations of the microprocessor by coupling the shifted memory address to the memory immediately after the microprocessor has finished booting, and continually coupling the shifted memory address to the memory for all subsequent normal operations of
25 the microprocessor.
35. (new) The electronic system of claim 34, wherein the memory is further for storing boot code for the microprocessor in the memory section, and the microprocessor is

further for booting utilizing the boot code stored in the memory section by coupling the first memory address to the memory before and during booting.

- 5 36. (new) The electronic system of claim 33, further comprising a register for storing a value being substantially equal to the size of the memory section to be protected; wherein the address translator is further for shifting the first memory address by the value stored in the register to thereby generate the shifted memory address; and after updating contents of the memory section,
- 10 the size of the memory section to be protected is changed to a new size; the register is further for storing a new value corresponding to the new size of the memory section to be protected; and the address translator is further for shifting the first memory address by the new value stored in the register to thereby generate a new shifted memory address.
- 15 37. (new) The electronic system of claim 36, wherein the memory section is further for storing updated boot code for the microprocessor.
- 20 38. (new) An electronic system comprising:
a microprocessor;
a memory being coupled to the microprocessor, the memory having a memory section of a particular size to be protected;
an address translator for generating a shifted memory address space of the memory, the shifted memory address space being shifted by an amount being
- 25 substantially equal to the size of the memory section to be protected to thereby move the memory section to be protected outside of the shifted memory address space;
wherein all memory accesses by the microprocessor access the memory utilizing

shifted memory addresses being within the shifted memory address space when it is desired to prevent the memory section from being accessed by the microprocessor.

39. (new) The electronic system of claim 38, wherein the address translator is further
5 for preventing the memory section from being accessed during normal operations of the microprocessor by coupling the shifted memory addresses of the shifted memory address space to the memory immediately after the microprocessor has finished booting and by continually coupling the shifted memory addresses to the memory for all subsequent normal operations of the microprocessor.

10 40. (new) The electronic system of claim 39, wherein the address translator is further for shifting an original memory address space of the memory by the amount being substantially equal to the size of the memory section to be protected to thereby generate the shifted memory address space;
15 the memory is further for storing boot code for the microprocessor in the memory section; and
the microprocessor is further for booting utilizing the boot code stored in the memory section by coupling un-shifted memory addresses in the original memory address space to the memory before and during booting.

20 41. (new) The electronic system of claim 38, further comprising:
a register for storing a value being substantially equal to the size of the memory section to be protected;
wherein the address translator is further for shifting an original memory address
25 space of the memory by the value stored in the register to thereby generate the shifted memory address space; and
after updating contents of the memory section,
the size of the memory section to be protected is changed to a new size;

the register is further for storing a new value corresponding to the new
size of the memory section to be protected; and
the address translator is further for shifting the original memory address
space of the memory by the new value stored in the register to
5 thereby generate a new shifted memory address space.

42. (new) The electronic system of claim 41, wherein the memory section is further for
storing updated boot code for the microprocessor.

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